Data Analysis of Measurements

Application on defects engineering

Semiconductor devices II - EE-567
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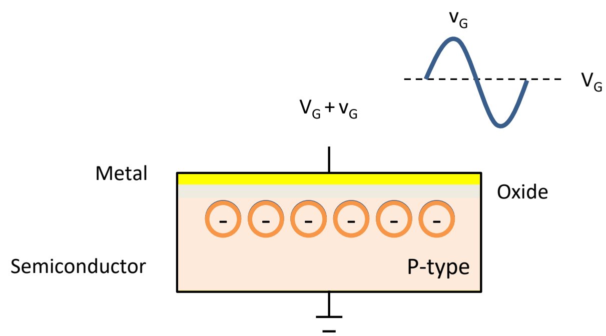
Outline

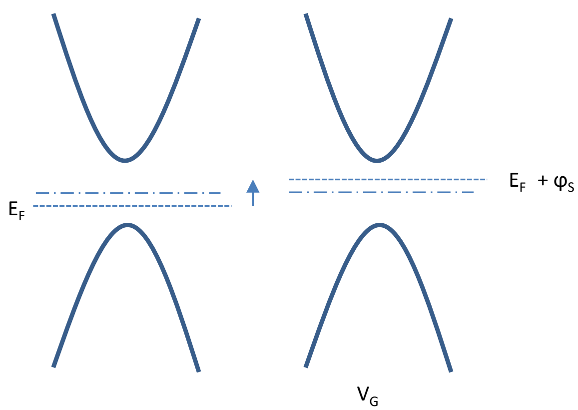
1. Review of CV Measurements
2. Defects on 2D Materials
3. Defect Modelling
4. Experimental Data
5. What to do?

1. Review of Defect Probing by CV Measurements

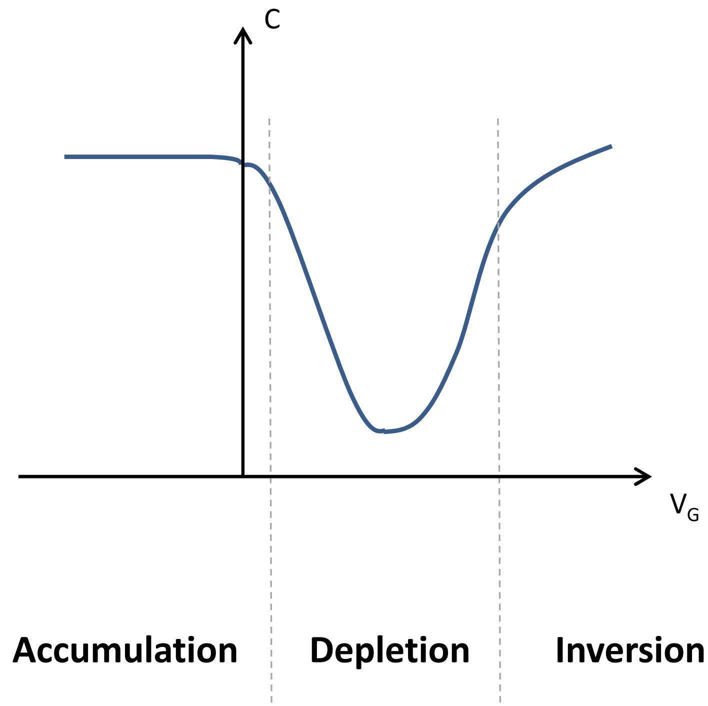
C-V Measurement Setup



The biasing probes the DOS



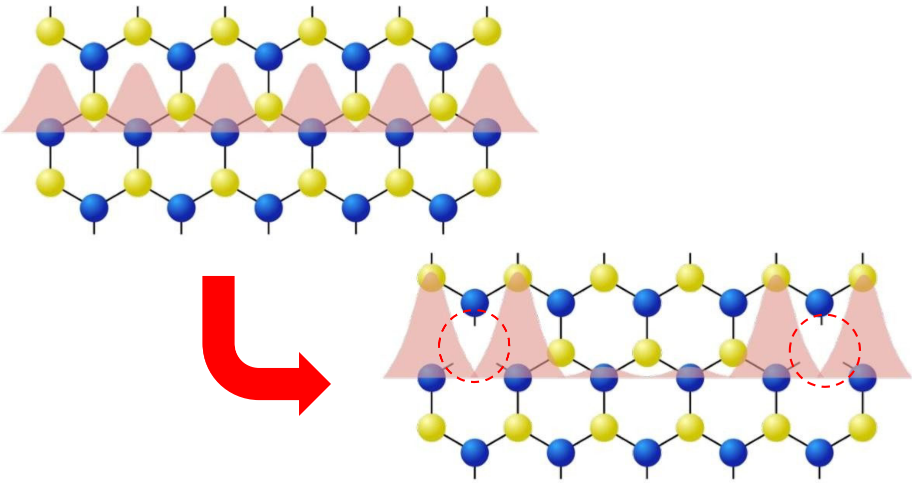
C-V Measurement

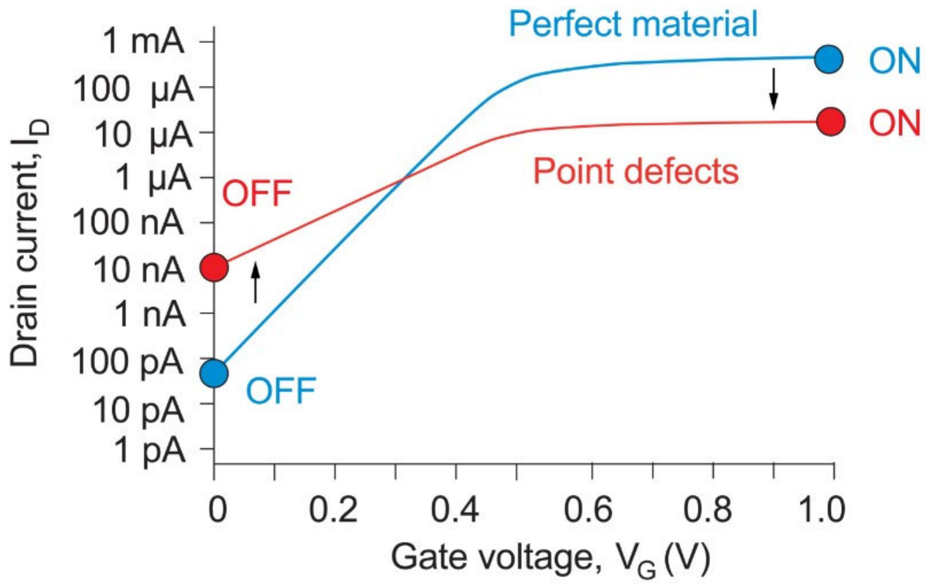


2. Defects on 2D Materials

2.1. Why (unwanted) defects are bad?

- **Reduce I_{ON}**
- **Increase I_{OFF}**
- **Reduce SS**
- **Slow Response**
- **Hysteresis**
- **Noise**





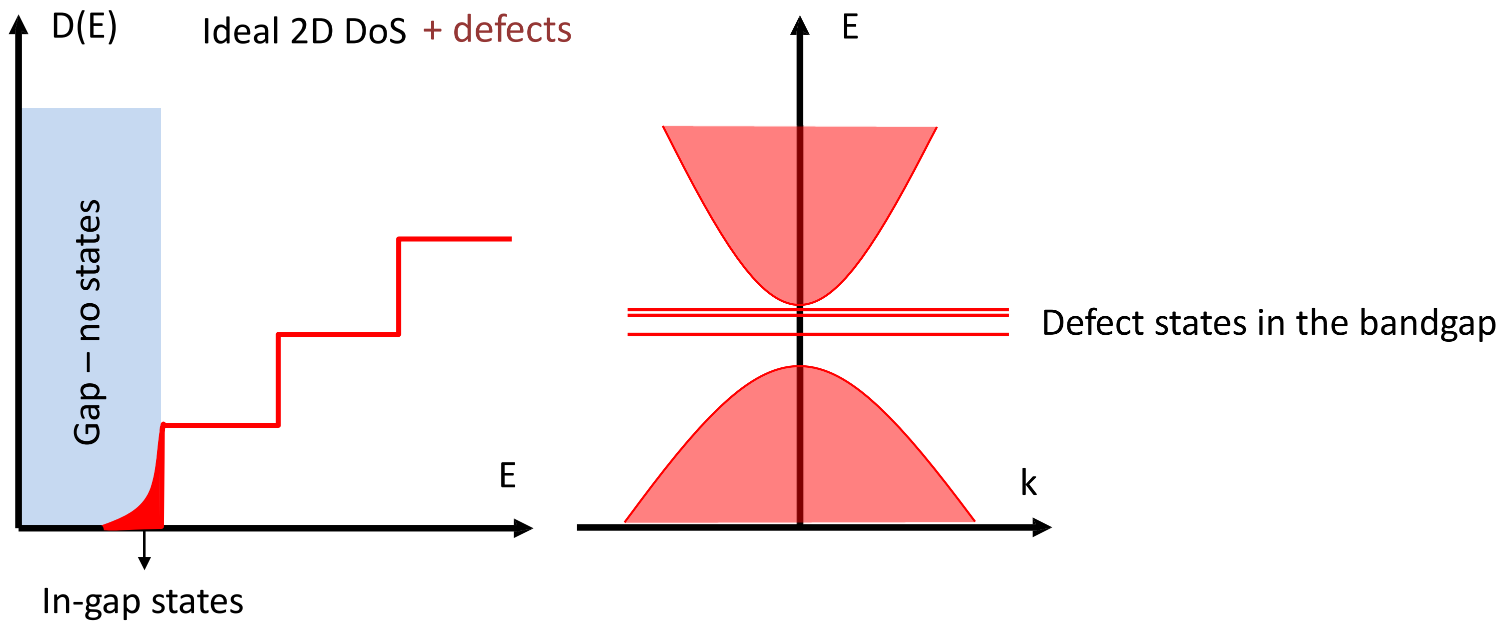
Localized wavefunctions

See slides from last lecture

2. Defects on 2D Materials

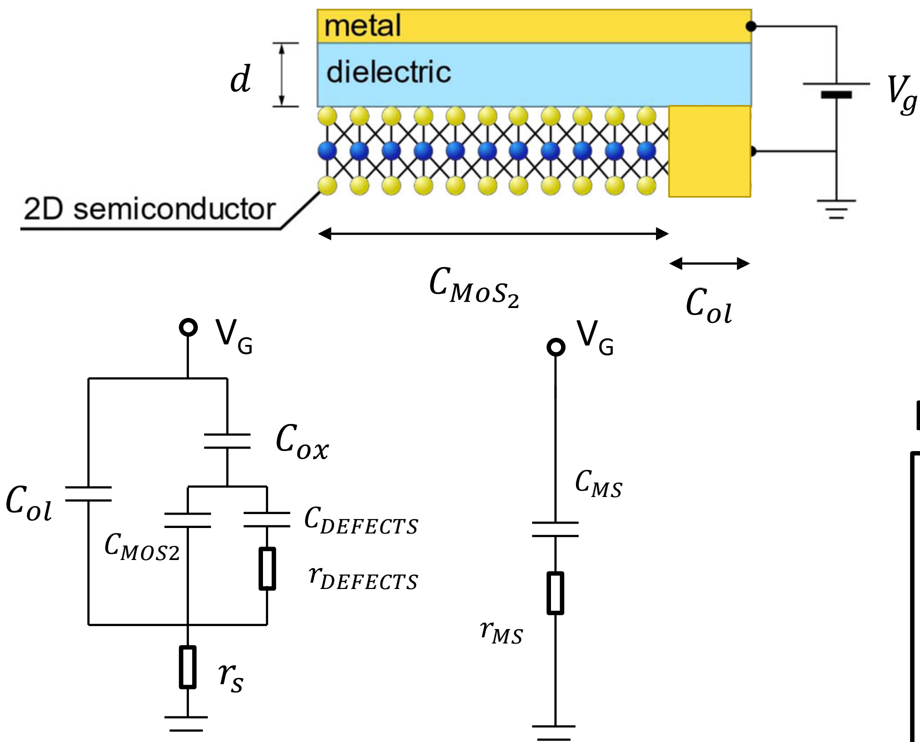
2.2. How defects look like in the band diagram

How to experimentally observe this?



2. Defects on 2D Materials

2.3. CV Measurements on 2D Materials



Modelling — Measurement

We measure the capacitance between the top and bottom contacts - C_{TOT}

We have several contributions to C_{TOT}

- Geometric capacitance (oxide)
- MoS_2 **quantum capacitance**
- Overlap of contacts

Modelled as a series of capacitors in series/parallel

Parameters

$$C_{TOT} = C_{ol} + \left(\frac{1}{C_{MoS_2}} + \frac{1}{C_{ox}}\right)^{-1}$$ is the total measured capacitance

$$C_{ox} = \frac{\epsilon\epsilon_0 A}{d}$$ is the geometrical capacitance

$$C_{MoS_2} = e^2 \cdot D(E)$$ is the quantum capacitance of MoS2

Quantum capacitance

Change of gate voltage: shift of channel potential U→ change in electron density

What is the relation between V_g and U?

For a **metal** you have **infinite DoS** – no need to raise energy to put more electrons in the channel

For a **SC** you have **a finite DoS** (+Pauli exclusion principle): to add more electrons you need to fill higher states

You can model this effect as an additional capacitance in your device

Since capacitances add in series, the smaller one dominates!

See also: https://www.youtube.com/watch?v=jSlVRmsiXuk

Luryi, S. Quantum capacitance devices. Applied Physics Letters 52, 501–503 (1988).

It is well known that a grounded metal plate completely shields the quasistatic electric fields emanating from charges on one side of the plate from penetrating into the other side. Thus, in a three-plate capacitor, illustrated in Fig. 1(a), application of a voltage to the node 1 changes the electric field only in the space filled with the dielectric ϵ_1. The situation is different if the middle plate Q is made of a *two-dimensional* (2D) metal, like the electron gas (2DEG) in a quantum well (QW) or an inversion layer. In this case, quite generally, the field due to charges on plate 1 partially penetrates through Q and induces charges on plate 2. As will be shown below, the capacitance C_{tot} seen at the node 1 is given by the equivalent circuit of Fig. 1(b), where C_1 and C_2 are the geometric capacitances:

$$C_i = \frac{\epsilon_i}{4\pi d_i}, \quad i = 1,2, \tag{1}$$

and C_Q the "quantum capacitance" per unit area:

$$C_Q = \frac{g_v m e^2}{\pi \hbar^2} = g_v \frac{m}{m_0} \times 6.00 \times 10^7\ \mathrm{cm}^{-1}. \tag{2}$$

Here m is the effective electron mass in the direction perpendicular to the QW plane, and g_v is the valley degeneracy factor.[1] Thus defined, C_Q coincides with the strong-inversion limit of the so-called inversion-layer capacitance, discussed by Nicollian and Brews[2] and other authors[3] in connection with the carrier-density fluctuations induced by interface charges in a metal-oxide-semiconductor (MOS) system. The quantum capacitance is a consequence of the Pauli principle, which requires an extra energy for filling a QW with electrons. In the classical limit, $\hbar \to 0$ or $m \to \infty$, one has $C_Q \to \infty$, and the capacitances C_2 and C_Q drop out, as they should. For MOS structures on a Si (100) surface, one has $g_v = 2$ and $m = m_l = 0.98 m_0$, so that $C_Q \gg C_1 \equiv C_{oxide}$ at all realistic oxide thicknesses. On the other hand, for a small m one can expect interesting effects when C_Q becomes comparable to the geometric capacitances. Partial penetration of an external field through a highly conducting 2DEG allows the implementation of several novel high-speed devices. Before discussing these devices, it may be worthwhile to go through a derivation[4] of the above equivalent circuit and Eqs. (1) and (2).

Let σ_1, σ_2, and σ_Q be the charge densities, respectively, on electrodes 1 and 2 and in the quantum well. The neutrality condition $\sigma_1 + \sigma_2 + \sigma_Q = 0$ can be written in the form

$$\sigma_2 = -\sigma_1 \sin^2(\phi), \tag{3a}$$

$$\sigma_Q = -\sigma_1 \cos^2(\phi), \tag{3b}$$

where ϕ is a variational parameter to be determined by minimizing the total energy E_{tot} of the system. The latter includes the field energies

$$E_i = \int_0^{d_i} \frac{\epsilon_i F_i^2\, dx}{8\pi} = \frac{2\pi d_i \sigma_i^2}{\epsilon_i}, \quad i = 1,2, \tag{4}$$

where $F_1 = 4\pi\sigma_1/\epsilon_1$ and $F_2 = -4\pi\sigma_2/\epsilon_2$ are the electric fields in regions 1 and 2, and the Fermi-degeneracy energy

$$E_Q = \pi\hbar^2\sigma_Q^2/2g_v m e^2. \tag{5}$$

(Corrections due to electron interaction[1] have been neglected.) Varying $\delta E_{tot}(\phi) = 0$, we find

$$\tan^2(\phi) = \hbar^2\epsilon_2/4mg_v d_2 e^2 \equiv C_2/C_Q, \tag{6}$$

which proves the equivalent circuit of Fig. 1. In particular, the charge induced on the ground metal plate equals

$$\sigma_2 = -\sigma_1[C_2/(C_2 + C_Q)]. \tag{7}$$

For possible applications an important consideration is by how much does the electrostatic potential Φ_Q of the QW vary in response to a variation of the voltage on electrode 1, at fixed voltages on the QW and electrode 2. This can be described by an "ideality factor,"

$$n \equiv \left(\frac{\partial \Phi_Q}{\partial V_1}\right)^{-1}_{V_Q - \mathrm{const}} = 1 + \frac{C_Q + C_2}{C_1}. \tag{8}$$

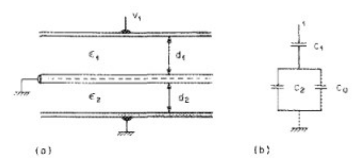
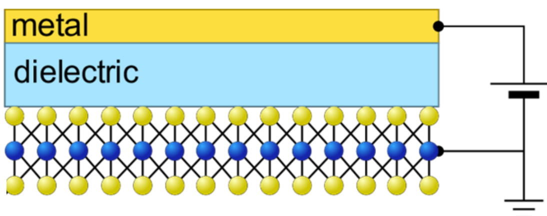


FIG. 1. (a) Schematic illustration of a three-plate capacitor in which the middle plate represents a two-dimensional metal. The space between the plates is assumed filled with dielectrics of permittivity ϵ_1 and ϵ_2. (b) Equivalent circuit for the capacitance seen at node 1.

3. Modelling of defects

3.1. CV Measurements on 2D Materials



Metal: infinite DoS

1L-MoS_2: 2D DoS

We do not consider Valence band since MoS2 is normally n-type

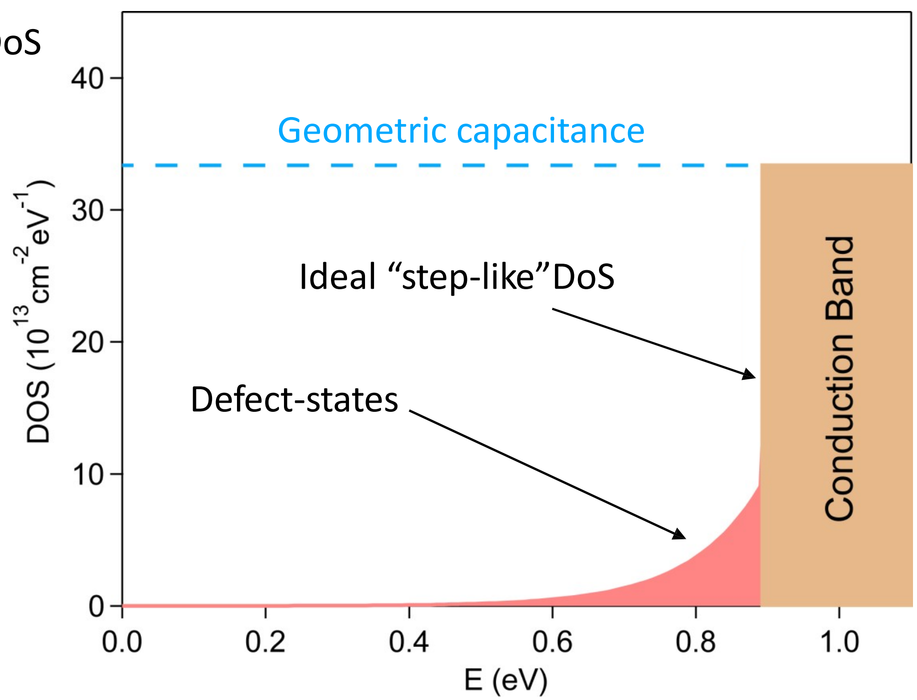
Capacitance: Quantum + defects contribution

$$C_{g-ch} = \frac{\partial Q_{ch}}{\partial V_G}$$

→ Charges in MoS_2 channel

$$Q_{ch} = e \cdot N = e \cdot \int_{-\infty}^{+\infty} f(E - eV_{ch}) \cdot D(E) \cdot dE$$

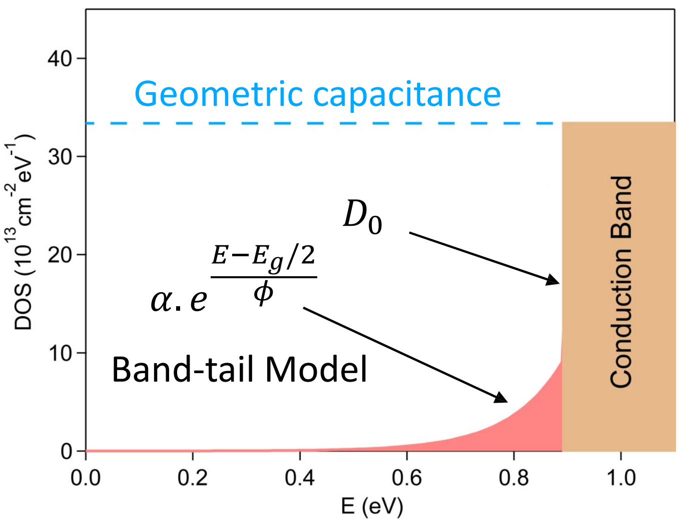
Density of states

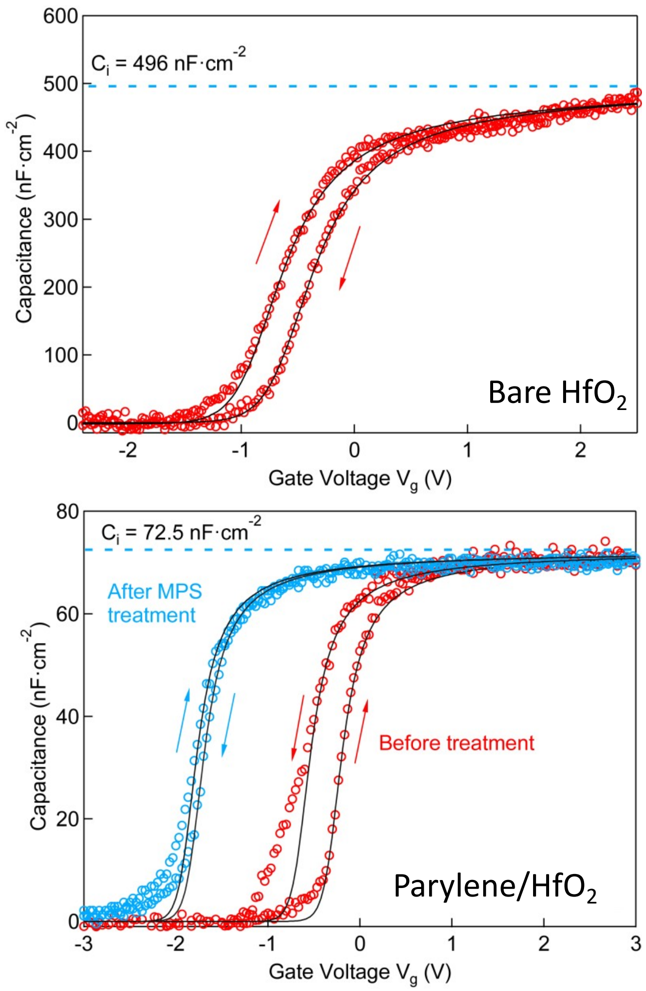


3. Modelling of defects

3.2. Model of defect DOS

$$D(E) = \begin{cases} \dfrac{2\, m^*}{\pi \hbar^2} & \text{If } E \leq E_C \\ \alpha\, e^{\frac{E - E_g/2}{\phi}} & \text{If } E > E_C \end{cases}$$





3. Modelling of defects

3.2. Model of defect DOS

$$\Phi_M + V_{ox} = V_g - V_{ch} + \chi + \frac{E_g}{2}$$

$$V_{ox} = \frac{Q_{ch}}{C_{ox}}$$

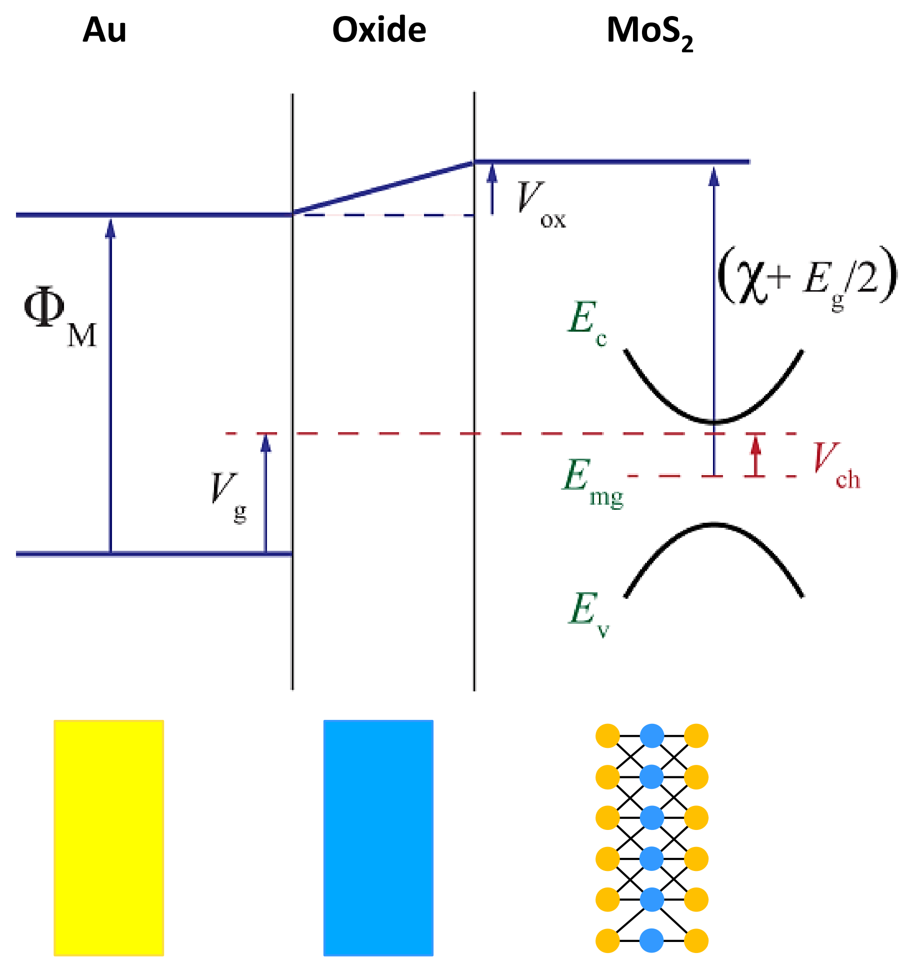
$$Q_{ch} = e \cdot N = e \cdot \int_{-\infty}^{\infty} f(E - eV_{ch}) \cdot D(E) \cdot dE$$

Note how V_{ch} appears in the integral equation:

$$\Phi_M + \frac{1}{C_i} \int f(E - eV_{ch}) D(E)\, dE = V_g - V_{ch} + \chi + \frac{E_g}{2}$$

$$C_{g-ch} = \frac{\partial Q_{ch}}{\partial V_g}$$

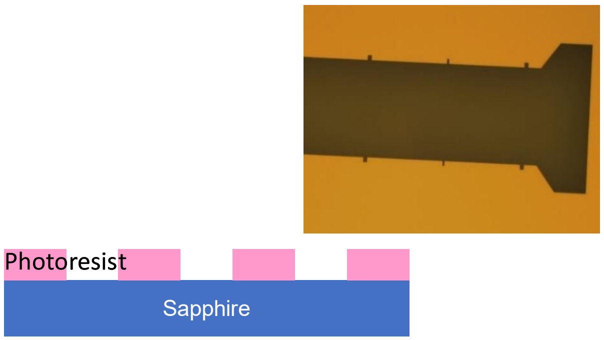
→ Experimentally measured quantity



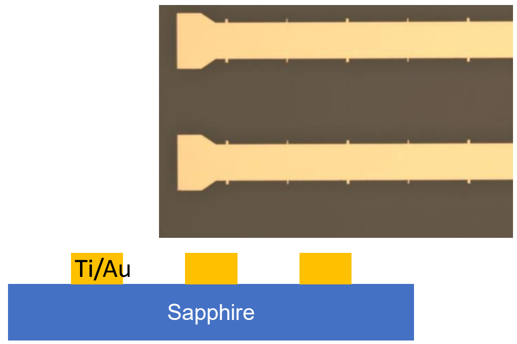
4. Experimental Data

4.1. Device Fabrication

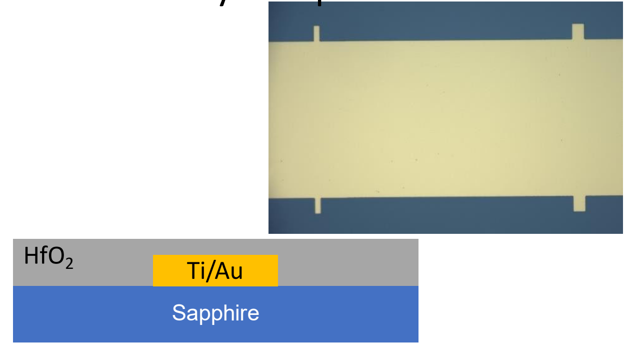
1. Gate Patterning



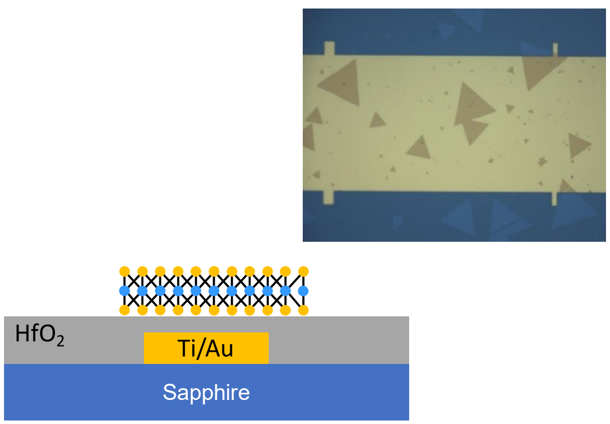
2. Gate Evaporation



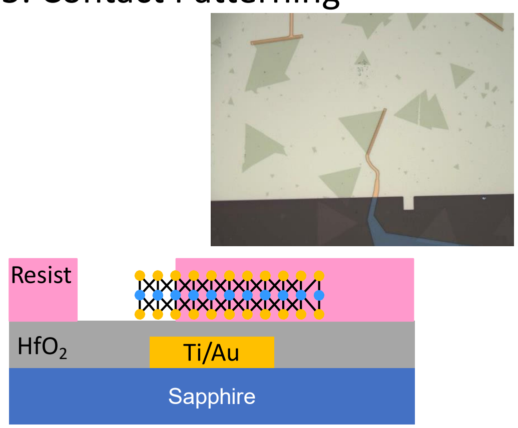
3. Atomic layer deposition



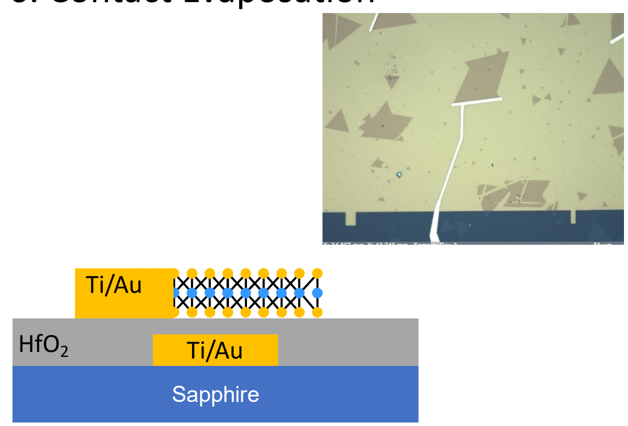
4. 2D Material Transfer



5. Contact Patterning

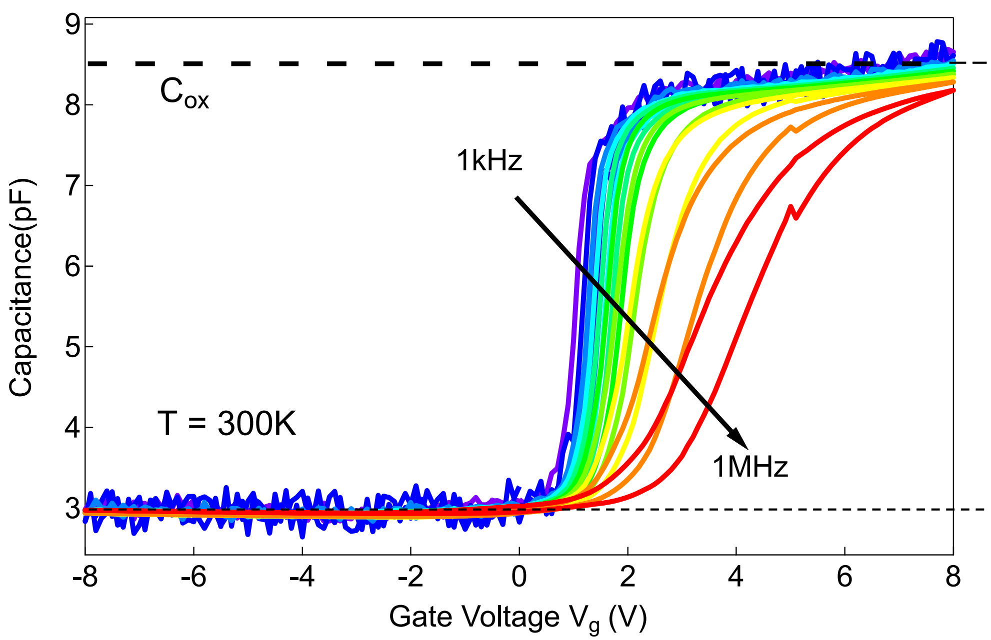


6. Contact Evaposation



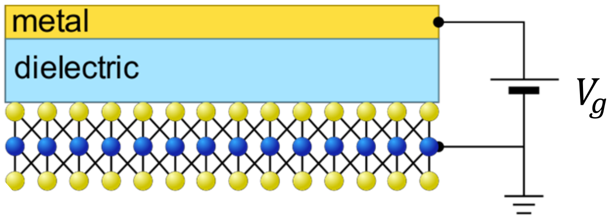
4. Experimental Data

4.2. Example of data



$$C_{max} = \frac{\varepsilon_{ox} \cdot (A_1 + A_2)}{t_{ox}}$$

$$C_{min} = \frac{\varepsilon_{ox} \cdot A_1}{t_{ox}}$$



The information is hidden. How to extract the useful information

4. Experimental Data

4.3. Finding the desired information

Experimental quantities:

- V_g applied voltage
- C_{TOT} measured capacitance
- C_i, C_{ol} can be extracted by calculations or by measuring empty devices

Physical quantities we want to find:

- α, ϕ parameters to describe the defects

$$C_{TOT} = C_{ol} + \left(\frac{1}{C_{MoS_2}} + \frac{1}{C_{ox}}\right)^{-1}$$

$$C_{g-ch} = \frac{\partial Q_{ch}}{\partial V_g}$$

$$Q_{ch} = e \cdot N = e \cdot \int_{-\infty}^{\infty} f(E - eV_{ch}) \cdot D(E) \cdot dE$$

$$D(E) = \alpha e^{\frac{E - E_g/2}{\phi}}$$ if $E > E_C$

5. What to do?

5.1 Procedure

1. Clean experimental data (background, systematic errors, etc…)

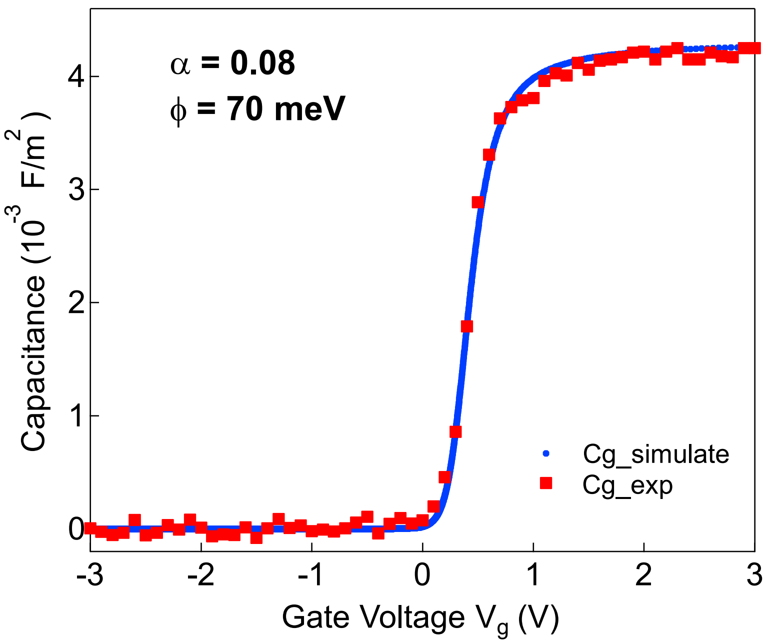
2. Write physical model

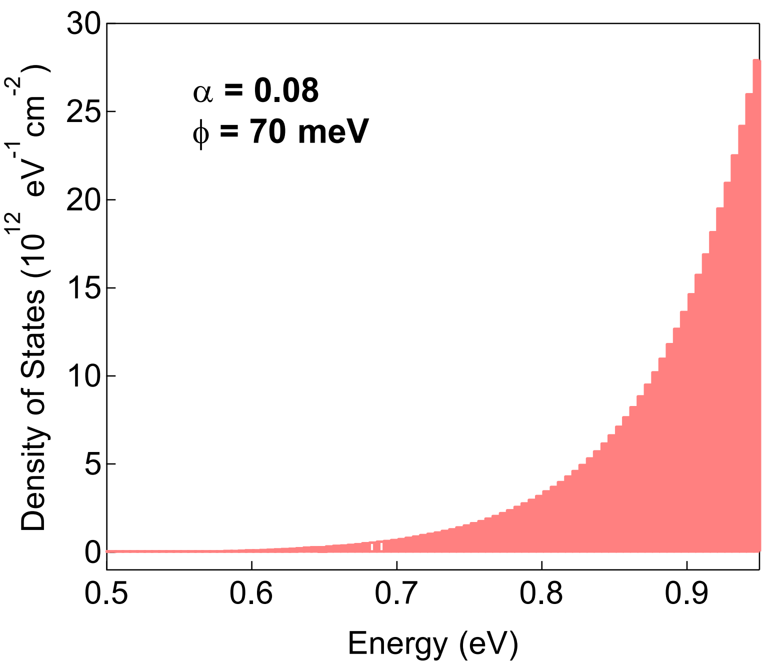
3. Fit the model to the data using a reasonable number of parameters

4. Check results

5. What to do?

5.2 What to expect in the end?





Code

- Write functions for Fermi distributions, DoS
- Integrate numerically to obtain the number of electrons in the channel as a function of the Fermi Energy

$$N = \int D(E) \cdot f(E - E_F)dE$$

- E_F is related to the channel voltage: $E_F = e \cdot V_{ch}$, so we can calculate the charge on the channel $Q_{ch} = e \cdot N$ as a function of V_{ch}
- BUT: V_{ch} is related to the applied gate voltage V_g through electrostatics equation $\Phi_M + \frac{Q_{ch}}{C_i} = V_g - V_{ch} + \chi + \frac{E_g}{2}$, so we need to find it

Code (2)

- We can use a loop to update V_{ch} from an initial guess until calculation converges:
  1. Initial guess: V_{ch}^0
  2. Calculate $Q_{ch}\left(V_{ch}^0\right)$
  3. Calculate $\Phi_M + \frac{Q_{ch}\left(V_{ch}^0\right)}{C_i} - V_g + \chi + \frac{E_g}{2} = V'_{ch}$
  4. Repeat step 2-3 with V'_{ch} to find V''_{ch}
  5. Iterate until $\Delta = |V_{ch}^{n+1}$- V_{ch}^{n}| is smaller than the desired precision

Code (3)

- ALTERNATIVE: in an un-physical but correct way, we can calculate Q_{ch}, V_g for a wide range of V_{ch} values and then take the ones corresponding to the V_g we use in our experiment!

- Once we have calculated Q_{ch}, V_g we calculate capacitance from $\frac{\partial Q_{ch}}{\partial V_g}$